SRI VASAVI INSTITUTE OF ENGINEERING & TECHNOLOGY

An Autonomous Institute
(Approved by AICTE, New Delhi & Permanently Affiliated to JNTUK Kakinada)
Accredited by **NBA** (ECE & CSE) **& NAAC**, An ISO 9001:2015 Certified Institute
Nandamuru, Pedana Mandal, Krishna Dist – 521369.

Date : 05-09-2026

M.TECH II SEMESTER (R25 REGULATION) REGULAR END EXAMINATIONS, SEPTEMBER - 2026
TIME TABLE

TIME : 10.00 AM TO 01.00 PM

BRANCH	28-09-2026 (MONDAY)	30-09-2026 (WEDNESDAY)	03-10-2026 (SATURDAY)	06-10-2026 (TUESDAY)	08-10-2026 (THURSDAY)
ECE (VLSI System Design - 61)	CMOS Mixed Signal Circuit Design (D2526101)	Physical Design Verification (D2526102)	VLSI Testing & Testability (D2526103)	SoC Design (D25261C3)	Quantum Computing (D25261D2)
CSE (Computer Science & Engineering - BA)	Machine Learning (D252BA01)	Natural Language Processing (D252BA02)	Introduction to Quantum Computing (D252BA03)	Generative AI (D252BAC2)	----------

NOTE:

i. Any Omissions or clashes in this time table may please be informed to the controller of examination immediately.
ii. The HOD's are requested to inform the Controller of Examination any other substitute subjects that are not included in the above time table immediately.

Controller of Examinations

Principal

Copy to:

1) Chairman, Secretary, Correspondent,
2) Executive Directors,
3) Controller of Examinations,
4) HODs – ECE & CSE,
5) Website, Main Notice Board, Student's Notice Board, Circular file & Exam Cell