SRI VASAVI INSTITUTE OF ENGINEERING & TECHNOLOGY

An Autonomous Institute
(Approved by AICTE, New Delhi & Permanently Affiliated to JNTUK Kakinada)
Accredited by **NBA** (ECE & CSE) **& NAAC**, An ISO 9001:2015 Certified Institute
Nandamuru, Pedana Mandal, Krishna Dist – 521369.

Date : 05-09-2026

M.TECH II SEMESTER (R23) SUPPLEMENTARY END EXAMINATIONS, SEPTEMBER - 2026
TIME TABLE

TIME : 10.00 AM TO 01.00 PM

BRANCH	28-09-2026 (MONDAY)	30-09-2026 (WEDNESDAY)	03-10-2026 (SATURDAY)	06-10-2026 (TUESDAY)
ECE (VLSI System Design - 61)	MIXED SIGNAL & RF IC DESIGN (M23EC21)	PHYSICAL DESIGN AUTOMATION (M23EC22)	Elective – III DESIGN FOR TESTABILITY (M23EC23A)	Elective – IV LOW POWER VLSI DESIGN (M23EC24C)
CSE (Computer Science & Engineering - 58)	BIG DATA ANALYTICS (M23CS21)	CRYPTOGRAPHY & NETWORK SECURITY (M23CS22)	Elective – III HUMAN COMPUTER INTERACTION (M23CS23C)	Elective – IV SOFTWARE TESTING AND QUALITY ASSURANCE (M23CS24C)

NOTE:

i. Any Omissions or clashes in this time table may please be informed to the controller of examination immediately.
ii. The HOD's are requested to inform the Controller of Examination any other substitute subjects that are not included in the above time table immediately.

Principal

Controller of Examinations

Copy to:

1) Chairman, Secretary, Correspondent,
2) Executive Directors,
3) Controller of Examinations,
4) HODs – ECE & CSE,
5) Website, Main Notice Board, Student's Notice Board, Circular file & Exam Cell