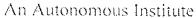
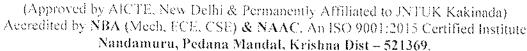


SRI VASAVE TOTITUTE OF ENGINEERING TECHNOLOGY







Date: 21-11-2023

<u>M.TECH I SEMESTER (R19 REGULATION) I MID EXAMINATIONS, NOVEMBER - 2023</u> <u>TIME TABLE</u>

TIME: 10.00 AM TO 12.00 AM

BRANCH	27-11-2023	28-11-2023	29-11-2023	30-11-2023	01-12-2023
	(MONDAY)	(TUESDAY)	(WEDNESDAY)	(THURSDAY)	(FRIDAY)
ECE (VESI System Design - 61)	CMOS ANALOG IC DESIGN (M23EC11)	CMOS DIGITAL IC DESIGN (M23EC12)	Elective – 1 VLSI TECHNOLOGY (M23EC13A)	Elective – II DEVICE MODELING (M23EC14A)	RESEARCH METHODOLOGY AND IPR (M23EC15)

NOTE:

- i. Any Omissions or clashes in this time table may please be informed to the controller of examination immediately.
- ii. The HOD's are requested to inform the Controller of Examination any other substitute subjects that are not included in the above time table immediately.

Controller of Examination

Principal

Copy to:

- 1) Chairman, Secretary, Correspondent,
- 2) Executive Directors,
- 3) Controller of Examination,
- 4) Hod's ECE & CSE,
- 5) Main Notice Board, Student's Notice Board, Circular file & Exam Cell